IN THE CLAIMS

Please amend the claims as follows:

1. (original) An apparatus comprising:

a memory array having a plurality of memory cells organized into a plurality of rows of multiple memory cells;

a marking buffer storing an indication of which rows of memory cells within the memory array are marked as having data to be preserved; and

a refresh logic to selectively refresh a row of memory cells if the row is marked in the marking buffer as having data to be preserved.

2. (original) The apparatus of claim 1, further comprising an interface to receive a command to carry out a refresh operation on a row of memory cells.

3. (original) The apparatus of claim 2, wherein the interface is configured to receive a value accompanying the command to carry out a refresh operation identifying a specific row of memory cells on which to selectively carry out the commanded refresh operation.

4. (original) The apparatus of claim 2, wherein the refresh logic further comprises a counter to provide a value identifying a specific row of memory cells on which to selectively carry out the commanded refresh operation in response to receiving the command to carry out a refresh operation on a row of memory cells.

5. (original) The apparatus of claim 1, further comprising:

an interface to receive a command to enter a reduced power state in which commands to carry out a refresh operation are not accepted from an external device; and

a counter to provide a value identifying a specific row of memory cells on which to selectively carry out a refresh operation in response to the passage of a predetermined interval of time.

6. (original) The apparatus of claim 1, wherein the marking buffer is comprised of one or more rows of memory cells comprising the memory array.

7. (original) An apparatus comprising:

a CPU;

a memory device having a plurality memory cells organized into a plurality of rows of multiple memory cells, and having an interface to receive a command to mark a row of memory cells as not having data to be preserved; and

a memory controller coupled to both the CPU and the memory device, and configured to transmit a command to the memory device to mark a row of memory cells as not having data to be preserved.

8. (original) The apparatus of claim 7, wherein the memory device further comprises a refresh logic that is configured to refrain from refreshing a row of memory cells marked as not having data to be preserved despite a request to refresh that row of memory cells.

9. (original) The apparatus of claim 8, wherein the memory device receives the request from the memory controller to refresh a specific row of memory cells.

10. (original) The apparatus of claim 8, wherein the refresh logic is comprised of a counter to provide an address of a row of memory cells to generate a request to refresh that row of memory cells.

11. (original) The apparatus of claim 7, wherein the memory controller is further configured to transmit a command to the memory device to mark a row of memory cells as having data to be preserved and the interface of the memory device is configured to receive the command to mark a row of memory cells as having data to be preserved.

12. (withdrawn) A method comprising:

transmitting a command to mark a row of memory cells within a memory device as having no data to be preserved; and

selectively refraining from carrying out a refresh operation on a row of memory cells within the memory device if the row of memory cells is marked as not having data to be preserved despite receiving a request to carry out a refresh operation on a row of memory cells.

13. (withdrawn) The method of claim 12, further comprising:

transmitting a command to mark a row of memory cells within the memory device as having data to be preserved; and

carrying out a refresh operation on a row of memory cells within the memory device if the row of memory cells is marked as having data to be preserved in response to receiving a request to carry out a refresh operation on a row of memory cells.

14. (withdrawn) The method of claim 12, wherein receiving a request to carry out a refresh operation on a row of memory cells comprises the memory device receiving a request transmitted by a device external to the memory device to carry out a refresh operation on a row of memory cells.

15. (withdrawn) The method of claim 12, wherein receiving a request to carry out a refresh operation on a row of memory cells comprises generating within the memory device a request to carry out a refresh operation on a row identified by an address generated by a counter within the memory device.

16. (withdrawn) The method of claim 15, wherein the generating of a request to carry out a refresh operation on a row takes place in response to the memory device receiving a command from a device external to the memory device to enter a reduced power state.

17. (withdrawn) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

transmit a command to a memory device within the electronic device to mark a row of memory cells within the memory device as having data to be preserved; and

writing data into the row of memory cells.

18. (withdrawn) The machine-accessible medium of claim 17, further causing the processor to: transmit a command to the memory device to mark a row of memory cells as not having data to be preserved.